A Hybrid Integration Strategy for Compact, Broadband and Highly Efficient Millimeter-Wave On-Chip Antennas

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***Abstract*—A novel hybrid integration strategy for compact, broadband and highly efficient mmWave on-chip antennas is demonstrated by realizing a hybrid on-chip antenna, operating in the [27.5-29.5] GHz band. A cavity-backed stacked patch antenna is implemented on a $600\,\mu\mathrm{m}$-thick silicon substrate by using air-filled substrate-integrated-waveguide technology. A hybrid on-chip approach is adopted in which the antenna feed and an air-filled cavity are integrated on chip and the stacked patch configuration is implemented on a high frequency PCB laminate that supports the chip. A prototype of the hybrid on-chip antenna is validated, demonstrating an impedance bandwidth of 3.7 GHz. In free-space conditions, a boresight gain of 7.3 dBi and a front-to-back ratio of 20.3 dB at 28.5 GHz are achieved. Moreover, the antenna is fabricated using standard silicon fabrication techniques and features a total antenna efficiency above 90 % in the targeted frequency band of operation. The high performance, in combination with the compact antenna footprint of $0.49\,\lambda_{min} \times 0.49\,\lambda_{min}$, makes it an ideal building block to construct broadband antenna arrays with a broad steering range.**

***Index Terms*—mmWave, On-Chip Antenna, Air-Filled Substrate-Integrated-Waveguide, High Efficiency, Broadband**

I. Introduction

As we embark on the road to the fifth generation of network technology (5G), countless challenges and opportunities emerge. To address the prime objectives of 5G, radical improvements are needed in the cellular network architecture [1]. Given that the cellular bands below $6\,\mathrm{GHz}$ cannot support the exponentially increasing demands, a key enabler to realize 5G is millimeter-wave (mmWave) communication. As such, 5G is likely to utilize much higher frequencies, up to mmWave and beyond [2]. On the one hand, one of the major challenges in implementing mmWave communication is overcoming the unfavorable propagation characteristics [3]. To conquer this hurdle, multi-antenna systems with adaptive beamforming will be indispensable [4], [5]. On the other hand, the exploitation of mmWave frequencies gives rise to smaller antenna footprints. This facilitates highly integrated radio units containing both the RF front-end and the antenna, thereby improving reliability and mitigating large interconnect losses [6]–[13]. In literature, two main strategies can be identified to realize these highly integrated RF solutions: antenna-on-chip (AoC) and antenna-in-package (AiP). Although both strategies are very promising, several critical issues remain. On the one hand, AoC solutions typically suffer from unfavorable electromagnetic material properties of bulk silicon substrates, resulting in poor antenna performance and substantial surface wave excitation [9]. On the other hand, AiP integration strategies face increased interconnect losses. These become more pronounced as the frequency of operation increases [9] and may be reduced by using flip-chip technology [11]. However, the inductive nature of the interconnects may lead to narrow-band performance [13]. Furthermore, in both integration strategies, utmost care should be taken to prevent electromagnetic interference (EMI) issues, due to inadequate shielding of the RF front-end [9].

In this letter, a novel hybrid integration strategy for compact, broadband and highly efficient mmWave on-chip antennas is demonstrated by realizing a highly-efficient hybrid on-chip antenna, operating in the [27.5-29.5] GHz band. A cavity-backed stacked patch antenna topology is selected and implemented in air-filled substrate-integrated-waveguide (AFSIW) technology. In order to achieve unprecedented overall AoC/AiP performance, a hybrid on-chip approach is adopted by implementing the antenna feed and a metallized air-filled cavity on chip and the stacked patch configuration on a Rogers $RO4350B^{®}$ laminate supporting the chip. The fabricated hybrid on-chip antenna exhibits a measured -10 dB-bandwidth of 3.7 GHz, a maximal gain of 7.3 dBi at $28.5\,\mathrm{GHz}$ and a total antenna efficiency larger than $90\,\%$ in the complete [27.5-29.5] GHz frequency band. Moreover, by leveraging a stacked-patch configuration, an antenna footprint of only 5.0 mm $\times$ 5.0 mm is obtained. Furthermore, a high isolation between the antenna and both the RF front-end and neighboring antennas is achieved by metallizing the air-filled cavity, thereby reducing EMI issues [9] and detrimental mutual coupling effects in antenna arrays [13], [14].

Many attempts to increase antenna efficiency have been described in literature, both for AoC [15]–[25] and AiP strategies [11], [13], [19]. Considering AoC strategies, micromachined patch antennas have been a popular antenna topology [8], [16], [17], [20]–[22], [26], achieving antenna efficiencies up to 95 %. However, these techniques usually result in an enlarged antenna footprint. Furthermore, high levels of mutual coupling [17] and/or susceptibility to EMI issues [15] were present due to a lack of metallization of the micromachined cavities. Other micromachined topologies have been reported as well [15], [18], [19], achieving equivalent radiation performance.

Yet, the aforementioned issues remain. Another common radiation enhancement technique is superstrate focusing [23]–[25], enabling easy integration with $0.13\,\mu\mathrm{m}$ SiGe or CMOS RF front-ends. However, the highest reported antenna efficiency is limited to 50 %. In conclusion, the AoC strategy typically leads to a constant trade-off between antenna efficiency, bandwidth and antenna footprint. In this respect, the AiP strategy allows achieving high antenna efficiencies within a small antenna footprint [11], [13], [19]. However, interconnects still remain an obstacle for AiP strategies [9] and, as such, hybrid integration strategies have been proposed to combine the best of both integration strategies, yielding high performance integrated antennas [10], [12]. Compared to [10], [12], our hybrid integration strategy reconciles the conflicting demands of high radiation efficiency, large bandwidth, small footprint and low interconnect losses by implementing the antenna feed and a metallized air-filled cavity on chip and exploiting the RF PCB laminate that supports the chip for the implementation of a stacked patch configuration. Furthermore, the use of AFSIW technology strongly reduces EMI issues, commonly encountered in AoC and AiP designs. The proposed hybrid integration strategy is validated by realizing a novel on-chip antenna. Its measured performance is compared with the current state-of-the-art in Table I, proving its excellent performance in terms of bandwidth, antenna efficiency and antenna footprint.

The remainder of this paper is organized as follows. In Section II, the hybrid on-chip antenna topology is proposed and the design evolution is discussed. Section III elaborates on the fabrication process and the relevant manufacturing tolerances. Simulation and measurement results are discussed in Section IV.

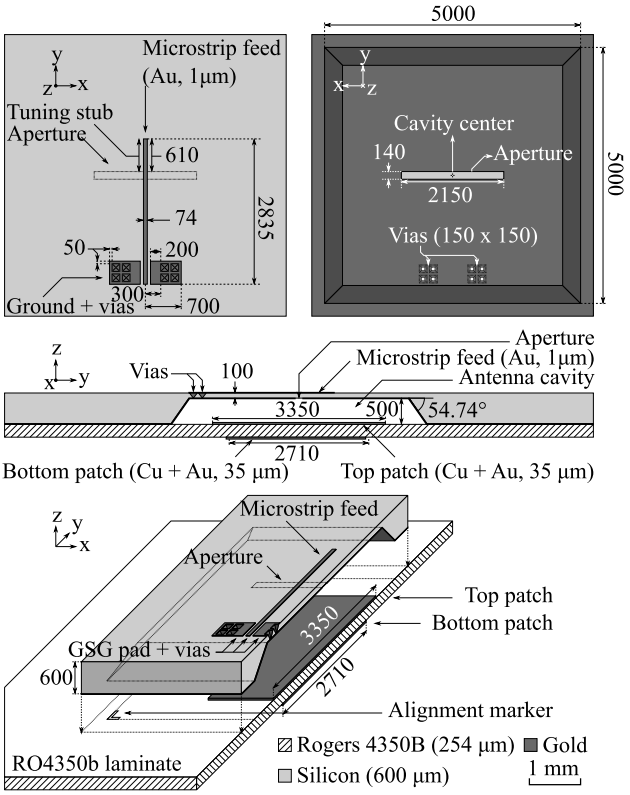


Figure 1: Structure of the hybrid on-chip antenna (dimensions in µm). Top left: top view; top right: bottom view; middle: cross-sectional view; bottom: 3D cross-sectional view. The rectangular top and bottom patch have dimensions $3350\,\mu\mathrm{m} \times 1800\,\mu\mathrm{m}$ and $2710\,\mu\mathrm{m} \times 3080\,\mu\mathrm{m}$, respectively.

II. Compact and highly-efficient hybrid on-chip stacked patch antenna

A linearly polarized, highly integrated antenna on silicon is designed for operation in the [27.5-29.5] GHz band, targeting an antenna footprint smaller than $5.450\,\mathrm{mm} \times 5.450\,\mathrm{mm}$ ($0.54\,\lambda_{min} \times 0.54\,\lambda_{min}$, with λ_{min} the free-space wavelength at $29.5\,\mathrm{GHz}$) for grating lobe-free beamsteering up to $\theta = \pm 60°$. Moreover, an antenna efficiency over 90 % is imposed in the complete bandwidth. Finally, a fabrication procedure that guarantees compatibility with CMOS and MEMS processes and, thus, allows mass production and scalability to even higher frequencies is strived for to remain competitive with current state-of-the-art solutions. To fulfill these stringent design requirements, a cavity-backed stacked patch antenna topology is adopted, as shown in Fig. 1. The backing cavity guarantees both a high antenna-to-integration platform isolation and reduces mutual coupling in arrays [14], while the stacked-patch configuration enables to satisfy the radiation and bandwidth requirements. To achieve the imposed total antenna efficiency, the antenna is implemented in AFSIW technology [27]–[29]. By removing the silicon substrate underneath the stacked patches and plating the newly exposed silicon surface, an AFSIW cavity is created. As a result, the electromagnetic fields of the stacked patch antenna reside in an air substrate for the most part and, hence, a low-loss antenna performance is achieved over a large bandwidth and surface wave excitation is strongly suppressed. Furthermore, by exploiting mode-bifurcation [29] in the stacked patch configuration, the antenna footprint of 5.0 mm × 5.0 mm remains below $0.54\,\lambda_{min} \times 0.54\,\lambda_{min}$, despite the use of AFSIW technology. As can be seen in Fig. 1, a hybrid on-chip antenna strategy is adopted. The antenna is constructed partially on chip and partially on a high-frequency PCB laminate, where the parts that need the highest accuracy are developed in silicon, making use of micro- and nanoscale fabrication technologies. The antenna cavity and feed structure are created in and on a $610\,\mu\mathrm{m}$ thick silicon wafer ($\epsilon_r = 11.9, \tan\delta = 0.0013$), respectively, whereas the patches are implemented on a $254\,\mu\mathrm{m}$ thick Rogers $RO4350B^{®}$ laminate ($\epsilon_r = 3.66, \tan\delta = 0.0031$), subsequently bonded to the silicon wafer with a non-conductive glue. On the one hand, the antenna feed structure is fabricated on-chip, making it compatible with standard silicon fabrication processes and thus, the implementation of the RF front-end can be both fully electrical [6], [7] or an opto-electrical hybrid [30], [31]. On the other hand, suspending the stacked-patch configuration on a Rogers $RO4350B^{®}$ laminate allows a radiation performance equivalent to AiP antennas, without frequency dependent interconnect losses. As such, our hybrid on-chip antenna approach minimizes interconnect losses and alleviates the trade-off

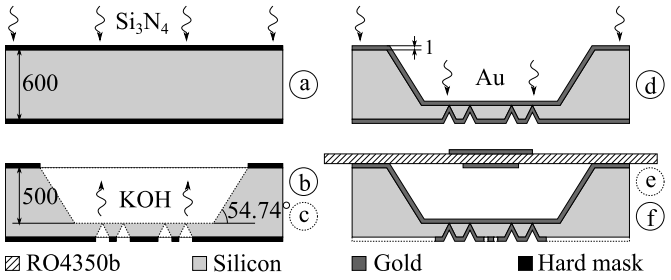


Figure 2: An overview of the fabrication process (dimensions in µm): (a) hard mask deposition, (b) hard mask patterning, (c) wet etch, (d) gold deposition, (e) gold patterning and (f) bonding.

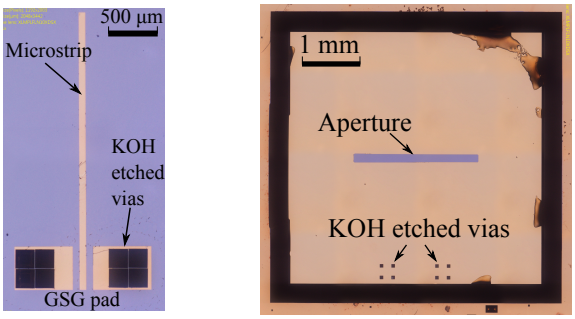
between bandwidth, efficiency and antenna footprint.

A 200 µm pitch ground-signal-ground (GSG) pad is used to enable antenna characterization with a probe, via a microstrip feed that excites the antenna by means of aperture coupling. Tuning the antenna feed dimensions, being the rectangular aperture and the tuning stub (see Fig. 1), allows for an optimization of the front-to-back ratio while still maintaining sufficient bandwidth. Moreover, leveraging aperture coupling provides adequate shielding between the antenna and feeding network, significantly mitigates parasitic radiation and benefits radiation pattern purity. Remark that the metallic traces on silicon are composed of gold and have a thickness of 1 µm, whereas the patches on the Rogers $RO4350B$® laminate are gold-plated copper traces and have a thickness of 35 µm. Both patches and the aperture in the cavity are centered around the cavity center. Furthermore, as the antenna cavity and vias are created with a low-cost potassium hydroxide (KOH) wet etch process, they exhibit sloped edges with a fixed angle of $54.74°$, as discussed in more detail in Section III. This is due to the (100) crystalline orientation of the silicon wafer. The proposed antenna is designed using the frequency domain solver of CST Microwave Studio. Its final dimensions are shown in Fig. 1.

III. Fabrication Process

The antenna is fabricated in the clean room facility of Ghent University. It is fully compatible with standard silicon fabrication processes, making it low cost and suitable for mass production. A high-resistivity (100) silicon substrate is used with a thickness of 600 µm and a reported resistivity of 40 Ωcm. The substrate is undoped, double sided polished, and contains a thin silicon oxide (SiO_2) layer of 400 nm on both sides. Using a chemical vapor deposition process, a 600 nm-thick silicon nitride (Si_3N_4) layer is deposited on both sides of the silicon wafer (Fig. 2(a)) to realize a hard mask for the wet etch. Next, the silicon wafer is cleaved into samples of 20 mm × 20 mm. The remainder of the processing is divided into the following steps: etching, metallization and bonding.

First, the antenna cavity and vias, described in Section II, are etched into the silicon samples. Thereto, a thin layer of TI prime [32] is spin coated onto the top side of the sample to promote adhesion of the photoresist in the next step. After the proper baking procedure, a 4 µm thick TI 35E [33] photoresist layer is spin coated on top of the TI prime layer and baked. Next, the SUSS MicroTec MA6/BA6 aligner is used to perform the photolithography step, where the image reversal technique [33] is adopted to pattern the photoresist. The Advanced Vacuum Vision 310 RIE is then used to transfer the pattern onto the hard mask with a plasma etching procedure, using a gas mixture of SF_6 and O_2. However, first, a thin TI 35E photoresist layer is coated on the backside of the sample to protect it during the plasma etching step. The cavity pattern is now transferred onto the hard mask of the silicon sample (Fig. 2(b)). Next, the same procedure is used to transfer the via patterns onto the hard mask on the sample backside. To ensure accurate positioning of the vias, backside alignment (with an accuracy of ±600 nm) is performed with the cavity corners as a reference. Finally, a wet etch procedure is performed using a 20% KOH solution. The etching solution is heated to 80 °C, resulting in a silicon etch rate of about 1.7 µm/min. The samples are submerged in the solution for 295 min, until a cavity depth of 500 µm is reached (Fig. 2(c)). Due to the (100) crystalline orientation of the silicon wafer, the edges are etched at an angle of $54.74°$ and, as such, the etching process of the vias stops automatically after the tip of its pyramidal shape is reached (Fig. 2(c)). After completing the etching process, a small portion of the cavity is punctured by the vias on the other side of the silicon sample. Lastly, the remainder of the hard mask is removed using a hydrofluoric acid (HF) solution.



(a) (b)

Figure 3: (a) Feed structure with GSG pad and (b) etched cavity with aperture of the on-chip stacked patch antenna.

In the second step, gold (Au) is deposited and patterned on both sides of the chip. First, a 10 nm layer of titanium (Ti) is predeposited on the sample backside by means of sputtering to act as an adhesive layer between the Si and Au. Afterwards, sputtering is applied to deposit a 1 µm-thick layer of Au (Fig. 2(d)). Next, an 8.8 µm-thick layer of AZ9260 positive resist [34] is applied to pattern the metal on the backside of the silicon sample during the photolitography step. After developing the sample in a 1:2 AZ400K [35] water solution, the feed structure of the antenna is finished (Fig. 2(e)). Next, the same procedure is performed for the top side of the sample to create the metal cavity and the feeding aperture. Backside alignment is again performed to guarantee accurate alignment of the different antenna features. A fabricated on-chip antenna prototype is shown in Fig. 3.

In the final step, the metallized silicon sample is bonded to a $RO4350B$® laminate, supporting a stacked patch structure. To this end, a 9 μm-thick layer of Cyclotene 3022-57 [36] is spin coated on the substrate. By using the alignment markers on the

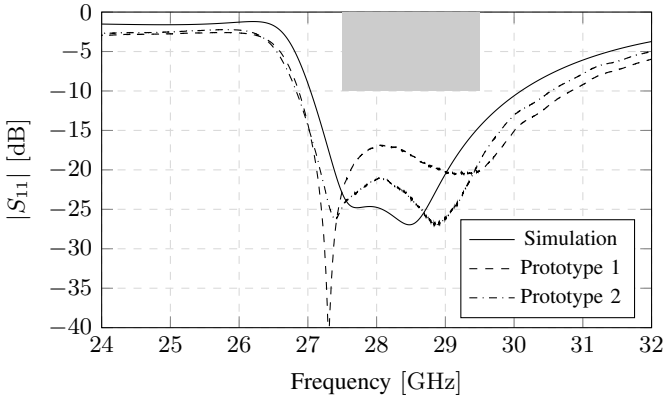


Figure 4: Simulated and measured magnitude of the reflection coefficient ($|S_{11}|$) w.r.t. $50\,\Omega$.

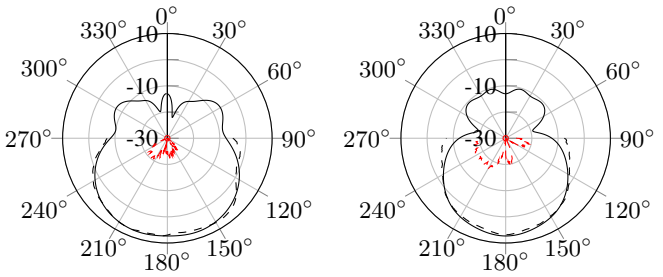


Figure 5: Simulated (solid) and measured (dashed), co-polarized (black) and cross-polarized (red) antenna gain at 28.5 GHz. (a) yz-plane (E-plane), (b) xz-plane (H-plane).

superstrate (Fig. 1), the chip and PCB laminate are aligned by means of a Finetech Pick and Place bonder (with an accuracy of ± 1 µm). After alignment, the chip and substrate are pressed together while being heated to $150\,^{\circ}\mathrm{C}$. After a heating period of $20\,\mathrm{min}$, the antenna is finished (Fig. 2(f)). A fabricated on-chip antenna prototype is shown in Fig. 3. Note that, in future array configurations some excess silicon can be placed at the edges of the chip, to provide sufficient bonding surface between the superstrate and chip.

IV. Simulation and Measurement Results

The reflection coefficient and far-field performance of the antenna prototypes are measured in the mmWave Anechoic Chamber [37] at Eindhoven University of Technology (TUe). This fully automated system, with a $1\,\mathrm{m}$ diameter and a $0.5\,\mathrm{m}$ height, is equipped with a probing setup that allows both back-side and front-side probing and is operational up to $90\,\mathrm{GHz}$. In this letter, backside probing is performed using a GSG-200 Picoprobe and a Keysight N5247A PNA-X Microwave Network Analyzer for both the reflection coefficient and far-field measurements. A SOLT calibration is performed to measure the scattering parameters of two prototypes, making use of a CS-5 calibration substrate [38]. For measurement purposes, the patch-supporting $RO4350B$® laminate is sized 4 cm $\times$ 4 cm. The excess $RO4350B$® laminate is used to install the antenna inside the anechoic chamber on top of a Rohacell ($\epsilon_r = 1.05, \tan\delta = 0.0034$) antenna mount.

The simulated and measured $|S_{11}|$ w.r.t. $50\,\Omega$ of the hybrid on-chip antenna and the prototypes are shown in Fig. 4. Two resonance peaks are visible, because of the two stacked patches, resulting in a measured and simulated bandwidth of 3.7 GHz and 3.1 GHz, respectively. A good agreement between simulated and measured radiation patterns (co- and cross-polarization) in the yz- and xz-plane at 28.5 GHz can be seen in Fig. 5. A simulated boresight gain of 6.64 dBi, 7.27 dBi and 7.38 dBi is achieved at 27.5 GHz, 28.5 GHz and 29.5 GHz, respectively. The corresponding measured gain is 6.62 dBi, 7.08 dBi and 7.12 dBi, respectively. This results in a total antenna efficiency of 92.7 %, 90.9 % and 90.4 % at those frequencies. Furthermore, a front-to-back ratio of 20.3 dB is obtained at the center frequency and an axial radio

Table I: Comparison of current work to the state-of-the-art.

	Technique	**f [GHz]**	**BW [%]**	η **[%]**	**A** [$\lambda \times \lambda$]
[17]	µMachining	135.0	8.90	80.0	0.81×0.81
[18]	µMachining	60.0	11.80	90.0	0.61×0.95
[19]	µMachining	143.0	13.90	76.0	0.95×0.95
[22]	µMachining	34.5	4.00	95.0	1.15×1.15
[24]	Superstrate	93.0	8.50	50.0	0.70×0.50
[19]	AiP	143.0	6.90	89.0	0.38×0.38
[11]	AiP	60.0	8.80	85.0	2.60×2.60
[13]	AiP	29.0	5.00	N.A.	0.23×0.23
[10]	Hybrid	60.0	12.60	73.0	0.33×0.16
[12]	Hybrid	68.0	5.70	96.7	0.16×0.28
This	**Hybrid**	**28.5**	**13.00**	**90.9**	$\mathbf{0.49 \times 0.49}$

over 20 dB within the 3 dB beamwidth of over 65° in both planes, is realized. Table I compares the proposed hybrid on-chip antenna with the state-of-the-art in terms of fractional bandwidth (BW), antenna efficiency (η) and antenna footprint (A). The antenna footprint is expressed in a fraction of the wavelength at the highest frequency of operation. It can be seen that the presented antenna enables excellent performance with respect to to the state-of-the-art, when considering the combination of bandwidth, efficiency and antenna footprint.

V. Conclusion

A novel hybrid integration strategy for mmWave antennas is demonstrated by realizing an on-chip AFSIW cavity-backed stacked patch antenna, featuring excellent performance in terms of radiation efficiency, broadside gain and bandwidth. Measurements report a total antenna efficiency over 90 %, a minimal boresight gain of 6.6 dBi and sufficient bandwidth to cover the [27.5-29.5] GHz band. Moreover, the compact antenna footprint (5.0 mm $\times$ 5.0 mm) in combination with the large beamwidth ($> 65°$) and high antenna-to-integration platform isolation, makes the proposed antenna element an attractive building block for multi-antenna systems with beam-steering capabilities.

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